Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] What is claimed is:

1.A memory address decoding method for determining if a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding address using the binary system, the method comprising:

making the corresponding address in a section with greater size smaller than the corresponding address in a section with smaller size;

bbuilding asingle bit-pattern for each section from all corresponding addresses; and

comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine the given address is located in one of the sections based on the comparison.

[c2] 2.The memory address decoding method of claim 1 wherein the sections are a plurality of memory modules.

[c3] 3.The memory address decoding method of claim 1 wherein the single bit-pattern is built for each section, the bit-pattern consisting of all common bits of the cor-

responding addresses in each section.

[c4] 4.The memory address decoding method of claim 1 wherein if the comparative bits of the given address do not match the bit-pattern bit in any section, the given address is not located in the section, otherwise the given address is located in the section.

[c5] 5.The memory address decoding method of claim 1 wherein the sections of same size can be swappable.

[c6] 6.The memory address decoding method of claim 1 wherein the corresponding addresses in each section increase or decrease in sequence so that the difference between one corresponding address and its previous corresponding address will be a fixed value.

[c7] 7.The memory address decoding method of claim 1 wherein the size of each section is a power of 2.

[c8] 8.Amemory address decoding method for determining whether a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding address using the binary system, the method comprising:
sorting the sections by size so as to make the corresponding address of the section with greater size smaller

than the corresponding address of the section with smaller size, and if after ssorting, thesize of a first section is equal to the size of a second section, the first and the second sections capable of being swapped;
building a single bit-pattern for each section from all corresponding addresses; and
comparing if at least one comparative bit of the given address matches those in any of the bit-patterns so as to determine in which one of the sections the given address is located based on the comparison.

[c9] 9. The memory decoding method of claim 8 wherein the sections are a plurality of memory modules.

[c10] 10. The memory decoding method of claim 8 wherein the single bit-pattern is built for each section, the bit-pattern consisting of all common bits of the corresponding addresses in each section.

[c11] 11. The memory decoding method of claim 8 wherein if the comparative bits of the given address do not match the bit-pattern bit in any section, the given address is not located in the section, otherwise the given address is located in the section.

[c12] 12. The memory decoding method of claim 8 wherein the corresponding addresses in each section increase or

decrease in sequence sso thatthe difference between one corresponding address and its previous corresponding address will be a fixed value.

[c13] 13. The memory decoding method of claim 8 wherein the size of each section is a power of 2.

[c14] 14. A control circuit of memory address decoding for determining whether a given address is located in one of a plurality of sections, each section having a plurality of memory units and each memory unit having a unique corresponding address, the corresponding address using the binary system, the control circuit comprising:
an access module for receiving the given address;
a sorting module for making the corresponding address of the section with greater size smaller than the corresponding address of the section with smaller size, and if the size of a first section is equal to the size of a second section, the first and the second sections are capable of being swapped; and
a comparing module for building a bit-pattern for each section based on its corresponding addresses and sending a plurality of comparison signals after comparing the given address with those of each bit-pattern.

[c15] 15. The control circuit of claim 14 further comprising a logic module responsible for receiving the comparison

signals and sending a decoding result to determine the given address is located in one of the sections.

[c16] 16. The control circuit of claim 14 wherein the sections are a plurality of memory modules.

[c17] 17. The control circuit of claim 14 wherein the single bit-pattern is built for each ssection inthe comparing module, the bit-pattern consisting of all common bits of the corresponding addresses in each section.

[c18] 18. The control circuit of claim 14 wherein the comparing module comprises a plurality of comparing units, each comparing unit comprising a plurality of first level AND gates, a plurality of XOR gates, and a second level AND gate, each of the first level AND gates having two inputs for respectively receiving a mask bit generated from the bit-patterns and an associated bit of the given address, each of the XOR gates having two inputs for respectively receiving the output of one of the first level AND gates and a standard address generated from the bit-patterns, the inputs of the second level AND gate being connected to the outputs of the XOR gates and thereby sending out the comparison signals.